SCAN CLOCK CIRCUIT AND METHOD THEREFOR

Abstract of the Disclosure

Embodiments of the present invention relate generally to scan clock waveform generation. One embodiment utilizes global and local circular shift registers to provide a series of shift/capture pulses at a manageable frequency for the tester and launch pulses that are phase shifted in order to provide for at-speed testing. Therefore, scan test patterns may be shifted in or out of state elements at lower frequencies as compared to the normal operating frequency of the integrated circuit being tested, while still allowing for at-speed testing. An alternate embodiment utilizes a circular shift register in combination with static storage devices and waveform generators to provide the shift/capture pulses and launch pulses. Embodiments of the present invention also allow for clock inversion where the clock and clock bar signals are dependent during normal mode and independent during scan test mode.